IN THE CLAIMS

1. (original) A computer processor comprising:

a main memory for storing programs and data associated with said programs;

a plurality of first processing units for processing said programs and said associated data, each said first processing unit including a local memory exclusively associated with said first processing unit;

a second processing unit for controlling said processing of said programs and said associated data by said first processing units, said second processing unit being operable to direct any one of said first processing units to process one of said programs by directing the transfer of said one program and data associated with said one program from said main memory to the local memory exclusively associated with said one first processing unit and instructing said one first processing unit to initiate processing of said one program, said one first processing unit thereafter processing said one program and said data associated with said one program from said local memory exclusively associated with said one first processing unit.

2. (original) The processor of claim 1, wherein said main memory is a dynamic random access memory.

3. (original) The processor of claim 1, wherein said main memory includes a plurality of memory locations, each said memory location including a memory segment exclusively associated with said memory location.

4. (original) The processor of claim 3, wherein each said memory segment stores status information indicating the status of data stored in said memory segment's associated memory location, the identity of a first processing unit and a memory address.

5. (original) The processor of claim 4, wherein said status information indicates the validity of said data stored in said memory segment's associated memory location, said identity indicates the identity of a particular one of said first processing units and said memory address indicates a storage location within the local memory exclusively associated with said particular one first processing unit.

6. (original) The processor of claim 1, wherein each of said first processing units is a single instruction multiple data processor.

7. (original) The processor of claim 1, wherein each of said first processing units includes a set of registers, a plurality of floating points units, and one or more buses connecting said set of registers to said plurality of floating point units.

8. (original) The processor of claim 7, wherein each of said first processing units further includes a plurality of integer units and one or more buses connecting said plurality of integer units to said set of registers.

9. (original) The processor of claim 1, further comprising an optical interface and an optical waveguide, said optical interface being operable to convert electrical signals generated by said processor to optical signals for transmission from said processor and to convert optical signals transmitted to said processor to electrical signals, said optical waveguide being connected to said optical interface for transmitting said optical signals.

10. (original) The processor of claim 1, wherein said local memories are static random access memories.

11. (original) The processor of claim 1, further comprising a rendering engine for generating pixel data, a frame buffer for temporarily storing said pixel data and a display controller for converting said pixel data to a video signal.

12. (original) The processor of claim 1, wherein the data associated with said one program includes a stack frame.

13. (original) The processor of claim 1, wherein each said first processing unit comprises a controller for directing, during said processing of said programs and said associated data, a transfer of further data from said main memory to the local memory exclusively associated with said first processing unit.

14. (original) The processor of claim 1, wherein said main memory comprises a plurality of memory bank controllers and a cross-bar switch for providing a connection between each of said first processing units and said main memory.

15. (original) The processor of claim 1, further comprising means for prohibiting each said first processing unit from reading data from, or writing data to, any of said local memories with which said first processing unit is not exclusively associated.

16. (original) The processor of claim 1, further comprising a direct memory access controller.

17. (original) The processor of claim 16, wherein said second processing unit directs said transfer of said one program and said data associated with said one program to the local memory exclusively associated with said one first processing unit by issuing a command to said direct memory access controller and, in response to said command, said direct memory access controller transfers said one program to the local memory exclusively associated with said one first processing unit.

18. (original) The processor of claim 17, wherein said one first processing unit directs the transfer of further data for processing said one program from said main memory to the local memory exclusively associated with said one first processing unit by issuing a command to said direct memory

access controller and, in response to said command, said direct memory access controller transfers said further data to the local memory exclusively associated with said one first processing unit.

19. (original) The processor of claim 18, wherein said one first processing unit directs a transfer of data resulting from said processing of said one program from the local memory exclusively associated with said one first processing unit to said main memory by issuing a command to said direct memory access controller and, in response to said command, said direct memory access controller transfers said resulting data from the local memory exclusively associated with said one processing unit to said main memory.

20. (original) A processing apparatus comprising

a main memory for storing programs and data associated with said programs;

one or more processor modules, each of said processor modules comprising a plurality of first processing units for processing said programs and said associated data, a plurality of local memories, each of said local memories being exclusively associated with a different one of said first processing units, a second processing unit for controlling said processing of said programs and said associated data by said first processing units, said second processing unit being operable to direct any one of said first processing units to process one of said programs by directing the transfer of said one program and data associated with said one program from said main memory to the local memory exclusively associated with said one first processing unit and instructing said one first processing unit to initiate processing of said one program, said one first processing unit thereafter processing said one program and said data associated with said one program from said local memory.

21. (original) The processing apparatus of claim 20, wherein the number of said plurality of first processing units for at least one of said processor modules is eight.

22. (original) The processing apparatus of claim 20, wherein the number of said first processing units for at least one of said processor modules is four.

23. (original) The processing apparatus of claim 20, wherein each of said processor modules comprises only one said second processing unit.

24. (original) The processing apparatus of claim 20, wherein each of said processor modules further comprises a direct memory access controller, said direct memory access controller being responsive to commands from said first processing units and said second processing unit to effect transfers of said programs and said associated data between said main memory and said local memories.

25. (original) The processing apparatus of claim 20, wherein each of said processor modules further comprises a local bus for providing communications among said first processing units and said second processing unit.

26. (original) The processing apparatus of claim 20, further comprising a module bus for providing communications among said processor modules.

27. (original) The processing apparatus of claim 20, further comprising a memory bus for providing communications between each of said processor modules and said main memory.

28. (original) The processing apparatus of claim 20, wherein each of said first processing units comprises a plurality of floating point units and a plurality of integer units.

29. (original) The processing apparatus of claim 20, further comprising one or more optical interfaces, each of said optical interfaces being operable to convert electrical signals

from said processor modules to optical signals for transmission from said processing apparatus and for converting optical signals transmitted to said processing apparatus to electrical signals.

30. (original) The processing apparatus of claim 20, wherein at least one of said processor modules further comprises a rendering engine for generating pixel data, a frame buffer for temporarily storing said pixel data and a display controller for converting said pixel data to a video signal.

31. (original) The processing apparatus of claim 27, wherein said memory bus comprises a plurality of memory bank controllers and a cross-bar switch for providing a connection between each of said processor modules and said main memory.

32. (original) The processing apparatus of claim 31, further comprising a second cross-bar switch for providing a connection between said main memory and devices external to said processing apparatus.

33. (original) The processing apparatus of claim 31, wherein said main memory comprises a plurality of banks and each of said memory bank controllers controls accesses to a different group of said banks.

34. (original) The processing apparatus of claim 33, wherein the number of said banks is sixty-four.

35. (original) The processing apparatus of claim 20, wherein the number of said processor modules is one.

36. (original) The processing apparatus of claim 20, wherein the number of said processor modules is two.

37. (original) The processing apparatus of claim 20, wherein the number of said processor modules is four.

38. (original) The processing apparatus of claim 20, wherein the number of said processor modules is eight.